Case Study on the Differences between EMI Resilience of Analog ICs against Continuous Wave, Modulated and Transient Disturbances

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***Abstract*—Transient disturbance signals are getting more and more attention lately (e.g. in the automotive industry). Electromagnetic compatibility (EMC) at IC level so far focused on continuous wave (CW) disturbances and how to deal with them, but transient phenomena were not thoroughly studied yet. In this exploratory paper, we perform a case study (based on a basic current mirror) in order to reveal the effects of transient disturbances (as compared to CW ones) and to determine what IC design techniques could be used to deal with them.**

Keywords—transient disturbance; EMC; EMI robustness; EMI tolerant circuits

I. INTRODUCTION

The electromagnetic compatibility (EMC) of integrated circuits has gained increasing importance over the last few decades [1]. EMC related issues have been alleviated at system level for quite some time. This includes EMC-aware printed circuit board (PCB) techniques like using external passive filtering, adding protective elements like chokes, shields, etc. This however comes with a high price, eventually increasing the bill of materials [2]. Moreover, external components like capacitors become inefficient at high frequencies (typically above 100 MHz) due to their large serial inductance [3]. Also, once the IC is produced, it is mostly unknown on which PCB it is going to be mounted, eventually bringing up the question whether ICs themselves must be insensitive to a certain amount of interference. And the answer is not surprisingly yes.

The typical IC-level electromagnetic interference (EMI) test range is 150 kHz to 1 GHz [1-3]. However, IC-level EMC standards will need to be revisited as many applications work at higher frequencies (e.g. RF communication working already beyond 60 GHz). This is of paramount importance in the sense that such high frequencies will largely increase the parasitic effects of IC-level interconnections that will act like inductors and even antennas, increasing the EMI susceptibility of the IC itself. Thus, IC-level EMC-aware design techniques will be no more a choice but rather an absolute necessity.

The International Electrotechnical Committee (IEC) has developed a series of standards that specify IC-level EMC test methods. The most well-known one is probably IEC 62132-4 [4] that specifies a direct power injection (DPI) test method. A frequently used specification for a global pin is 30 dBm. This can be translated into 40 Vpp interference immunity for a high impedance node or 20 Vpp for a 50 ohm matched network [3].

For EMI tolerant IC design techniques, several publications in the literature can be found [5-12]. In view of the aforementioned IEC 62132-4 [4], nearly all tests concerning EMI susceptibility of ICs have been made using single frequency (or narrow band) continuous sinusoidal signals within the specified frequency range of 150 kHz - 1 GHz. This previous research revealed the main interference mechanisms (resulting e.g. in DC offsets of operating points and output signals) and proposed a number of design rules and circuit techniques to mitigate the interference effects of these disturbances. Meanwhile, transient EMI phenomena have started to attract attention in many fields including the automotive industry where it has become a hot topic. However, to the best of our knowledge, transient disturbances, in contrast to continuous wave (CW) interferences, have not been studied deeply in the literature and it is hard to find scientific publications at IC level.

Aside from modulated signals, there has recently been a huge demand to establish certain protection requirements against transient disturbance signals (both in terms of keeping the functionality within specifications and avoiding physical damage). In case such disturbance signals are present at the pins of the IC, the question arises whether (1) the same mitigation techniques can be used as in the case of continuous wave DPI, (2) other existing techniques can be used, or (3) new ones need to be developed. The exploration of the answer to this question is the main driver of this paper.

In this paper, an exploratory analysis of the effects of transient disturbances on analog integrated circuits is performed. For comparison purposes, EMI disturbances ranging from very narrow-band ones (such as CW and amplitude modulated disturbances) up to very broad-band ones (similar to electrostatic discharge or ESD) are used.

One might think that design techniques that have been applied to cope with ESD pulses can also be applied for

transient disturbance signals. However, in terms of signal properties, there is a huge difference between CW signals and ESD pulses and different circuit design methodologies may need to be developed for transient signals that are somewhere in between in terms of amplitude and frequency. In most cases, clamping the disturbance can save the circuitry from physical damage caused by ESD. However, keeping the functionality within specifications or creating a fail-safe operation in such an event, is impossible with mere clamping. Thus, special treatments need to be made when handling such transient disturbance signals. In this respect, the effects of various types of disturbances should be investigated and appropriate design methodologies need to be developed for dealing with them. In this paper, a first attempt is made to further explore this point by using a current mirror case disturbed by various signals.

The paper is organized as follows. In section II, a current mirror case study is presented where one of the most catastrophic effects of EMI in ICs, namely DC shift, occurs. In this study, results are presented for CW, amplitude modulation (AM) and pulse signals. In section III, conclusions summarizing the work are drawn.

II. CASE STUDY

One of the most catastrophic effects of EMI in analog circuits is the DC shift phenomenon [2-3]. DC shift could also be named slope pumping here. What happens is that the disturbance signal that reaches a nonlinear circuit node, mixes with the intended signal and so introduces an additional DC term. This DC term can cause the operating point of the circuit to shift so much from the expected value that the original signal can no longer be recovered, eventually bypassing the normal operation of the circuitry. This is indeed problematic in the sense that conventional filtering mechanisms can no longer help cancelling out the disturbance signal. In this case study it is first illustrated how this occurs in a basic current mirror. Later in the study, the difference between CW and transient disturbance signals will be presented and it will also be demonstrated that in the transient case some techniques are suitable that are not so in the CW case, thereby supporting the claim that transient disturbances should indeed be studied in detail and that adapted methodologies need to be developed for robustness against such disturbance signals.

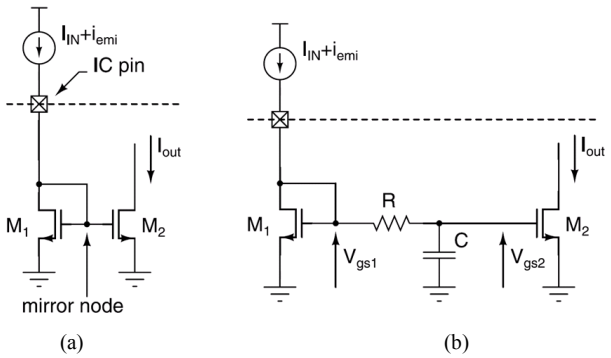

Fig. 1. (a) Classical current mirror; (b) RC low pass filtering applied at the mirror node.

In the left part of Fig. 1, a conventional current mirror is shown. In a 3.3V, 0.18µm CMOS technology, 10µA DC current is being mirrored. On top of the DC current, a CW 1 MHz sinus has been applied with various amplitudes from 10 µA to 50 µA as can be observed from Fig. 2. To filter out the 1 MHz disturbance, a basic RC filter is used with a corner frequency of 10 kHz to have an attenuation of 40 dB. As can be seen in Fig. 3, after filtering, due to the aforementioned DC shift phenomenon, the output current is heavily distorted as the interference amplitude goes high. The apparent conclusion is that, after the EMI has reached the nonlinear node of the circuitry (mirror node in this case), filtering is not a solution to mitigate the EMI.

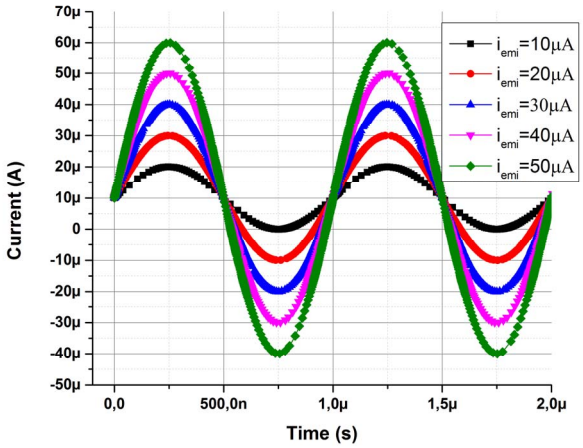

Fig. 2. Various amplitude EMI currents injected at the input.

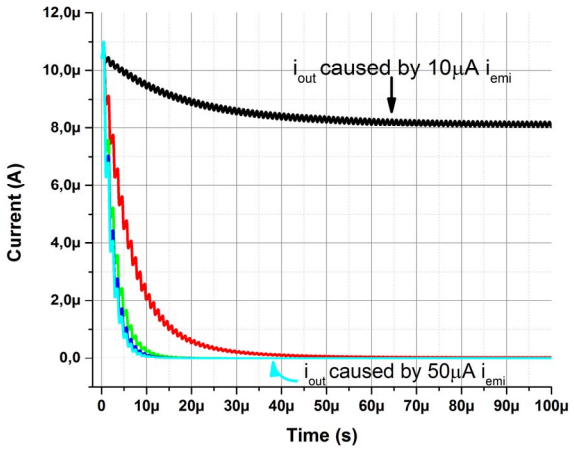

Fig. 3. Output current after CW injection at the input.

To determine a mathematical expression for the DC term, the mean value of the output transistor's gate-to-source voltage need to be derived. The following expression can be written:

$$\overline{V_{gs}} = Vt + \sqrt{\frac{I_{IN}}{\frac{\mu Cox}{2}\frac{W}{L}}}\left(1-\frac{1}{16}m^2-\frac{15}{1024}m^4-\frac{105}{16384}m^6\ldots\right) \quad (1)$$

where m is the ratio of i_{emi} to the DC current I_{IN}. Further details on the derivation of (1) can be found in [2].

As can be observed from (1), the expression inside the parentheses is causing the DC level to shift downwards. It is clear that when no EMI is present, this factor equals 1, meaning no DC shift is present. As also stated in [2], the amount of DC shift could be decreased by increasing the DC current which eventually increases the bandwidth of the circuitry. However, it will also increase the power consumption.

The IEC 62132-4 DPI test specification [4] states that the injected RF noise can also be amplitude modulated (AM). However, the peak power (P_{AMpeak}) and thus also the corresponding peak voltage (V_{AMpeak}) should remain the same [13]. The relation between their mean powers is stated in [4] as:

$$\overline{P_{AM}} = \overline{P_{CW}} \cdot \frac{2+m^2}{2(1+m)^2} \tag{2}$$

where m is the modulation index. Using a modulation index 1 yields $\overline{P_{AM}} = 0.375\overline{P_{CW}}$. If less mean power is being injected, as a result, less DC shift is intuitively expected. In this case, still keeping the disturbance frequency at 1 MHz, again 10µA DC current is being mirrored and with a peak amplitude of 10µA CW and AM signals are placed on top of the DC current with f_{mod}=10 kHz. After the application of the same RC filter, the output current is observed. As can be observed from Fig. 4, when the disturbance is an AM signal with the same peak amplitude as the CW signal, the overall DC shift is less which supports the average (mean) power approach stated above. During the instances where the disturbance amplitude is decreasing, the output DC value gets into a trend of recovering until the next increasing disturbance reaches the input node.

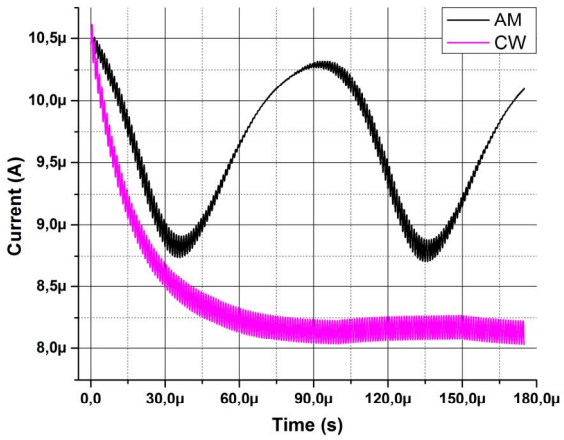

Fig. 4. Output currents in case of CW and AM disturbance.

As a next step, to analyze the case where a short-duration pulse is applied, the Fourier series expansion for a pulse train of trapezoidal pulses will be considered.

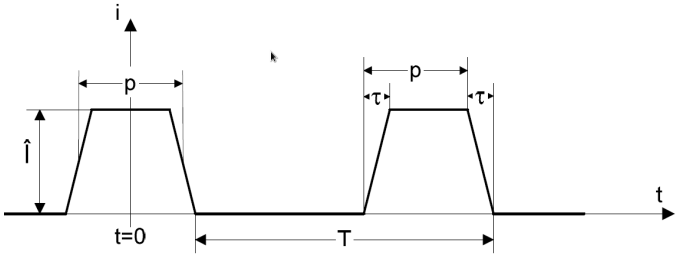

Fig. 5. Current waveform for a trapezoidal pulse train.

The Fourier expansion of the waveform shown in Fig. 5 is given by

$$i(t) = \frac{\hat{I}\,p}{T} + \sum_{n=1}^{\infty} I_n \cos\left(\frac{2\pi n t}{T}\right) \tag{3}$$

where $\hat{I}$ is the peak current value (A), T is the period (s), p is the pulse duration (s), τ is the transition time (s) and

$$I_n = \frac{2\hat{I}\,p}{T} \frac{\sin\left(\frac{n\pi\tau}{T}\right)}{\frac{n\pi\tau}{T}} \frac{\sin\left(\frac{n\pi p}{T}\right)}{\frac{n\pi p}{T}} \tag{4}$$

To ease the interpretation of (4), it can be deduced from it that the I_n coefficients are bounded by

$$|I_n| \le \frac{2\hat{I}\,T}{n^2\pi^2\tau} \tag{5}$$

Perhaps the most obvious observation is that the I_n coefficients will become negligibly small for large n (typically for n>T/τ). Another observation is that the mean power (and hence "disturbance strength") could become very low if p/T tends to zero. In fact, if T tends to infinity, the pulse train becomes equivalent with a single transient pulse.

What happens when the interference signal is not a CW signal but a pulse train is shown in Fig. 6. Here, a positive square pulse of 1 µs duration (with 10 ns rise and fall times) is applied on top of the same 10 µA DC current and the amplitude of the disturbance is swept. The pulse period (T) is chosen to be 100 µs. As can be seen from the figure, the circuit recovers, and the DC shift is far less compared to the CW case. Here it should be noted that there is of course a limit up to which the circuit can survive such a disturbance. In case of excessive positive or negative voltages on a transistor's nonlinear node, intrinsic pn junctions might open causing huge substrate currents to flow uncontrollably which could turn on latch-up mechanisms and other destructive effects. At this point, ESD protection or a similar clamping needs to be used. A simple example of such a protection is depicted in Fig. 7 where the excessive currents are diverted through the

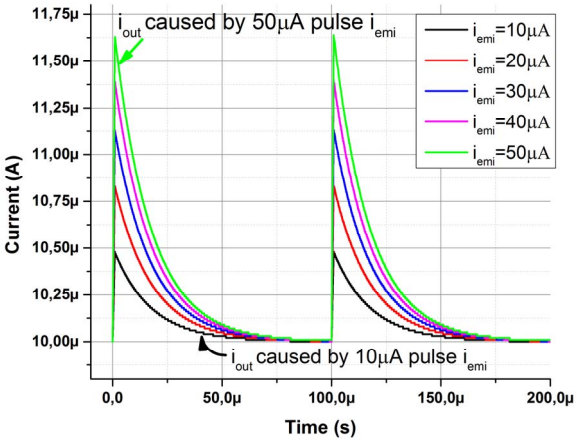

Fig. 6. Output current after the application of a pulse train of τ = 10 ns, p = 1 µs and T = 100 µs.

protection diodes D1 and D2, preventing latch-up or worse physical damages to the IC. Following is an example where a relatively excessive current pulse with an amplitude of 5 mA and a duration of 1 µs is applied to the mirror node. As clamping circuitry, Schottky diode arrays are used with sufficient current handling capacity to divert the interference. Fig. 8 depicts the output currents in such a case. Even without the clamping circuitry, thanks to the RC filter at the gates, the DC value of the actual current of interest is recovered. However, this can be deceiving since the node voltages must be taken into account in such an event. Fig. 9 depicts the gate (which is connected to the drain) voltage during excessive current pulse application. For this specific example, VDD = 3.3 V and the transistors are tolerant to 3.6 V. It is therefore apparent from the figure that without clamping, there is a good chance that the transistor will break down.

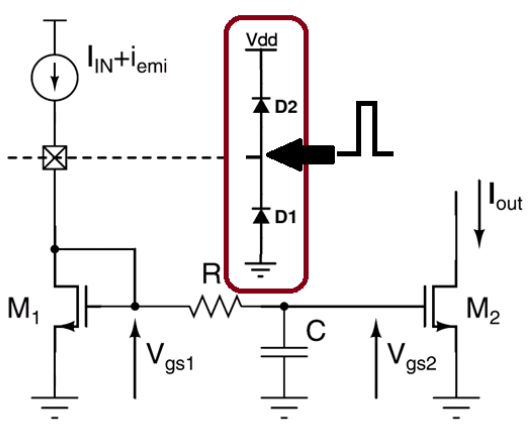

Fig. 7. Clamping circuitry for a transient pulse protection.

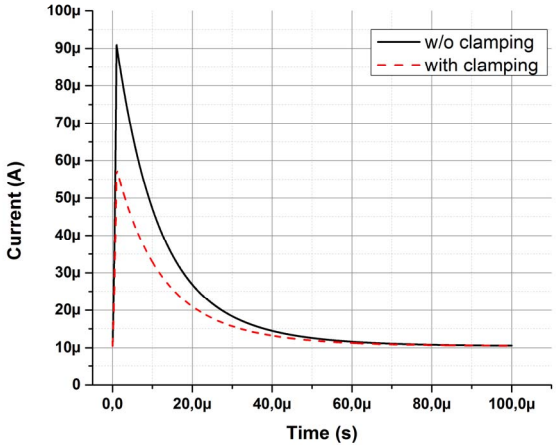

Fig. 8. Output currents with and without clamping for 5 mA positive current pulse event.

For sure the use of clamping should be studied carefully since if the clamping occurs when it should not, this would mean more nonlinearity, eventually causing more DC shift and even the bypassing of the normal operation of the circuitry.

Based on the above results, it looks likely that when it comes to transient disturbances, circuit techniques like basic filtering could still be used at nodes where it is not possible to do so for CW injection. As stated in [2], it is still a better idea to tackle the disturbance signal before it reaches a nonlinear node. However, there is an open window for the designer to still use filtering solutions when it comes to transient disturbances. Also, as mentioned in the previous section, due to the fact that the frequency range could be increased soon to a domain where IC tracks start to act like antennas, having filter usage possibility should clearly prove itself worthwhile.

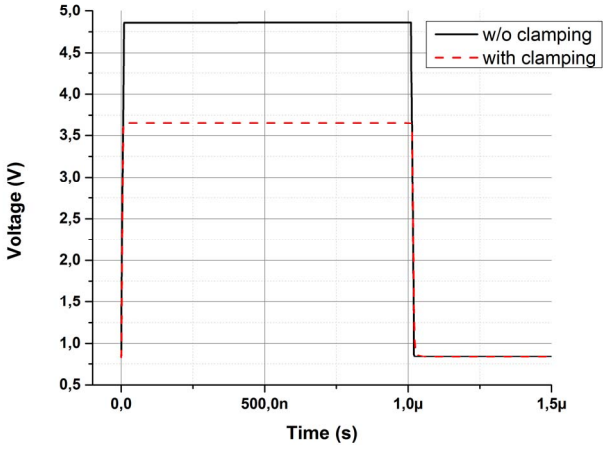

Fig. 9. Gate voltage of M1 during 5 mA positive pulse injection on top of 10 µA DC current.

III. Conclusion

A case study based on a conventional current mirror has been carried out in order to explore the differences between three RF disturbance signals, namely single-frequency CW, narrow-band AM and broad-band pulse disturbances. The findings obtained in this study, could be summarized as followed:

- The DC shift phenomenon is less of an issue for transient disturbances than for CW or AM ones.
- Filtering is still an option for transient disturbances whereas it does not work for CW disturbances.
- Clamping is an option, but care must be taken in order to not add more nonlinearity to the circuitry which could turn out to be catastrophic in terms of functionality.
- Up to some level duration is more important than amplitude for transient disturbances.
- It looks very challenging to combine adequate EMI resistance against both narrow-band and wide-band signals.
- For broadband transient disturbances there may be no more clear distinction between in-band and out-of-band disturbances.

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